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PTO/SB/08A (08-03)

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			<b>Complete if Known</b>		
			Application Number	09/880,734	
			Filing Date	June 12, 2001	
			First Named Inventor	Crosland, Andrew	
			Art Unit	2116	
Examiner Name	Tse W. Chen				
Sheet	1	of	2	Attorney Docket Number	15114-053500US

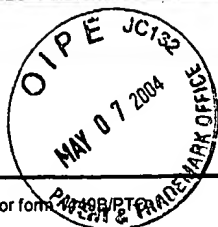
U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
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PTO/SB/08B (08-03)

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		<b>Complete if Known</b>			
		Application Number	09/880,734		
		Filing Date	June 12, 2001		
		First Named Inventor	Crosland, Andrew		
		Art Unit	2116		
		Examiner Name	Tse W. Chen		
Sheet	2	of	2	Attorney Docket Number	15114-053500US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
TWC	AO	DeHON, DPGA-Coupled Microprocessors: Commodity ICs for the Early 21st Century, Artificial Intelligence Laboratory, Massachusetts Institute of Technology, Cambridge, MA, IEEE, February, 1994, pp. 31-33	
TWC	AP	HAUSER, and WAWRZYNEK, University of California, Berkeley, "Garp: A MIPS Processor with a Reconfigurable Coprocessor," IEEE, April 1997, pp. 12-21.	
TWC	AQ	IBM Corporation, "Mixture of Field and Factory Programmed Logic Cells in a Single Device," IBM Technical Disclosure Bulletin, April 1995, pp. 499-500	
TWC	AR	NAGEL, "ACM Computing Surveys: Synergy Between Software and Hardware," Carnegie Mellon University, Department of Electrical Engineering and Computer Science, Pittsburgh, PA, December, 1996, pp. 1-3.	
TWC	AS	RAZDAN, and SMITH, "A High-Performance Microarchitecture with Hardware-Programmable Functional Units," Harvard University, Cambridge, MA, Digital Equipment Corporation, Hudson, MA, November, 1994, pp. 172-180.	
TWC	AT	WITTIG, and CHOW, "OneChip" An FPGA Processor With Reconfigurable Logic," Department of Electrical and Computer Engineering, University of Toronto, Ontario, Canada, IEEE, September, 1996, pp. 126-135.	
TWC	AU	WYNN, "In-Circuit Emulation for ASIC-Based Designs," Xilinx, Inc., VLSI Systems Design, October, 1986, pp. 38-39, and 42-45.	
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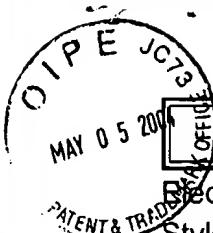
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## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18  
Stylesheet Version v18.0

Title of Invention	Embedded processor with watchdog timer for programmable logic						
Application Number:		09/880734					
Confirmation Number:		4950					
First Named Applicant:		Andrew Crosland					
Attorney Docket Number:		015114-053500US					
Art Unit:		2116					
Examiner:		Tse W Chen					
Search string:		( 5687325 or 6260087 ).pn.					
<b>US Patent Documents</b>							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
tw	1	5687325	1997-11-11	Web Chang			
tw	2	6260087	2001-07-10	Web Chang			
Signature							
Examiner Name				Date			
TSE CHEN				9/23/04			



ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18  
Stylesheet Version v18.0

Title of Invention	Embedded processor with watchdog timer for programmable logic
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Application Number: 09/880734  
Confirmation Number: 4950  
First Named Applicant: Andrew Crosland  
Attorney Docket Number: 015114-053500US  
Art Unit: 2116  
Examiner: Tse W. Chan  
Search string: ( 6467009 or RE34444 or 5970254 ).pn.



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US Patent Documents

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init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
<i>tlw</i>	1	6467009	2002-10-15	Winegarden			
<i>tlw</i>	2	RE34444	1993-11-16	Kaplinsky			
<i>tlw</i>	3	5970254	1999-10-19	Cooke			

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Sheet 1 of 1

## Complete If Known

Application Number	09/880,734
Filing Date	June 12, 2001
First Named Inventor	Crosland, Andrew
Group Art Unit	2819
Examiner Name	Unassigned
Attorney Docket Number	015114-053500US

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## U.S. PATENT DOCUMENTS


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## FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>3</sup>
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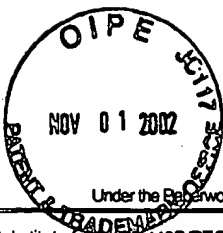
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tuc	01	"Triscend E5 Configurable System-on-Chip Family," Product Description from Triscend Corporation, January, 2000 (Version 1.00), pp. i-ii and 1-90.	
tuc	02	"Motorola Technical Developments," Magazine of Motorola, Inc., Vol. 39, September 1999, pp. i-vii and 77-80.	
tuc	03	"AT94K Series Field Programmable System Level Integrated Circuit," Advance Information Brochure of Atmel Corporation, December 1999, 6 pages.	
tuc	04	"CS2000 Reconfigurable Communications Processor Family Product Brief," Advance Product Information from ChameleonSystems, Inc., 2000, pages 1-8	
tuc	05	"Wireless Base Station Design Using Reconfigurable Communications Processors," Wireless Base Station White paper from ChameleonSystems, Inc., 2000, pages 1-8.	

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		Application Number	09/880,734
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Filing Date	June 12, 2001
		First Named Inventor	Crosland, Andrew, et. al.
		Art Unit	2819
		Examiner Name	To Be Assigned
		Attorney Docket Number	015114-053500US
Sheet	2	of	2

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
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<i>twc</i>	0015	AITKEN, R.C., and AGARWAL, V.K., "A Diagnosis Method Using Pseudo-Random Vectors Without Intermediate Signatures," Proc. of Int. Conf. on Computer-Aided Design (ICCAD), IEEE pp. 574-577 (1989).	
<i>twc</i>	0016	Altera "APEX 20K Programmable Logic Device Family Data Sheet," May 1999, 7 pages total.	
<i>twc</i>	0017	Altera "FLEX 10K Embedded Programmable Logic Family Data Sheet," May 1999, 7 pages total.	
<i>twc</i>	0018	Altera "FLEX 8000 Programmable Logic Device Family Data Sheet," May 1999, 5 pages total.	
<i>twc</i>	0019	Altera "IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices," August 1999, Application Note 39, 29 pages total.	
<i>twc</i>	0020	Altera "MAX 7000 Programmable Logic Device Family Data Sheet," May 1999, 6 pages total.	
<i>twc</i>	0021	GHOSH-DASTIDAR, J., and TOUBA, N.A., "A Rapid and Scalable Diagnosis Scheme for BIST Environments With a Large Number of Scan Chains," Proc. of IEEE VLSI Test Symposium, pp. 79-85 (2000).	
<i>twc</i>	0022	GHOSH-DASTIDAR, J., DAS, D., and TOUBA, N.A., "Fault Diagnosis in Scan-Based BIST using Both Time and Space Information," Proc. of International Test Conf., IEEE, pp. 95-102 (1999).	
<i>for</i>	0023	MC ANNEY, M.G. and SAVIR, J., "There is Information in Faulty Signatures," Proc. of International Test Conf., IEEE, pp. 630-636 (1987).	

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